

**REMARKS**

The Office Action dated July 30, 2003, has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto. Applicants respectfully note that no new matter has been entered through the above amendments. Claim 1 has been amended to more particularly point out and distinctly claim the subject matter of the invention. Claim 6 has been added. Support for the changes to claim 1 and claim 6 may be found in the present application at pages 99-108. Claims 1-6 are pending in the above-cited application and are respectfully submitted for consideration.

Claims 1 and 2 were rejected under 35 U.S.C. § 102(a) as being anticipated by *Muller et al.* (U.S. Patent No. 5,909,686 or *Muller '686*). Claims 3-5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Muller '686* in view of *Muller et al.* (U.S. Patent No. 6,119,196 or *Muller '196*). The above rejections, as may be reasserted against the claims as amended, are respectfully traversed according to the remarks that follow.

The present invention is directed to, according to claim 1, a network switch stack configuration. The configuration includes a first network switch comprising a plurality of data ports, a first stacking port, and a first CPU interface, a second network switch having a plurality of data ports, a second stacking port, and a second CPU interface and a common CPU connected to the first CPU interface and the second CPU interface. Additionally, the first stacking port and the second stacking port are communicatively connected, such that incoming packets on any of the plurality of data ports on the first

and second switches can be effectively switched to any of the plurality of data ports on either of the first and second network switches and the first and second switches add module headers to the incoming packets and the first and second stacking ports read the module headers to determine egress ports for the packets.

*Muller '686* is directed to a method and apparatus for providing hardware-assisted CPU access to a forwarding database. A switch fabric provides access to a forwarding database on behalf of a processor, and includes a memory access interface configured to arbitrate access to a forwarding database memory. The switch fabric includes interfaces for communicating with a CPU, shared memory, network ports and a cascading interface communicating with one or more switch elements.

*Muller '196* is directed to a method and apparatus for managing a buffer memory in a packet switch that is shared between multiple ports in a network system. The apparatus comprises a plurality of slow data port interfaces configured to transmit data at a first data rate between a slow data port and the buffer memory and a plurality of fast data port interfaces configured to transmit data at a second data rate between a fast data port and the buffer memory. A first level arbiter is coupled to the plurality of slow data port interfaces, where the first level arbiter chooses an access request of one the slow data ports and outputs the access request.

In the Office Action, it appears that the Office has taken a position that the cascading interface (225) of *Muller '686* is equivalent to the stacking ports recited in claim 1, in that it allows packets being passed between interconnected switching

elements. However, nothing in either *Muller '686* or *Muller '196* teaches that “the first and second switches add module headers to the incoming packets and the first and second stacking ports read the module headers to determine egress ports for the packets. Neither reference discloses any particular methodology associated with the cascading interface. As such, Applicants respectfully assert that any anticipation rejection of claim 1 over *Muller '686* and *Muller '196*, taken alone or in combination, would be improper for failing to teach all of the elements of invention as claimed.

In addition, Applicants also respectfully assert that claim 1 is also not rendered obvious by any of the prior art of record. There is no disclosure in the references of a module header or some equivalent structure that would provide the functionality recited in claim 1. Therefore, one of ordinary skill in the art would not have been motivated to modify any of the cited references to reach the claims of the present invention.

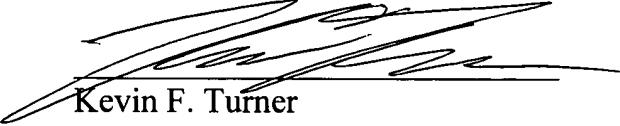
Thus, Applicants respectfully assert that any rejection of claim 1 over *Muller '686* and/or *Muller '196* would be improper for failing to teach or suggest all of the elements of that claim. On the basis of the above, independent claim 1 is respectfully asserted to be patentable, and as a consequence the dependent claims 2-6 are patentable as well. It is therefore respectfully requested that claims 1-6 be allowed and this application be allowed to pass to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by

telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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